Claim 27, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Soininen et al.(Pub. Appl. '293)

each of these rejections is respectfully traversed. It is initially noted that claim 32 is listed on the Office Action Summary form as being rejected; however, no rejection is presented for claim 32, which like claim 21 is generic to all the Specie I-IV, since claim 32 broadly includes the limitation of claim 21 of "a barrier metal film of a metal whose conductivity will not be lost when the metal is oxidized or of a conductive metal oxide." Further, claim 32 is not addressed as being withdrawn and should not have been since like claim 21 it is generic to all specie. Please note that the Applicants' Response to Restriction, Election of Species Requirement of June 25, 2002 states that claims 22 and 24-27 are readable on the elected specie of Figure 1A-1E, i.e., using a Ru barrier layer in a through-hole; while "at least claim 22 (sic 21) is generic to all species."

The presently claimed invention of independent claims 21 and 35 relates to the using "a metal whose conductivity will not be lost when the metal is oxidized" and "a conductive metal oxide" as a barrier layer, respectively. Therefore, when the barrier layer and seed layer are sequentially deposited, even when the barrier layer is exposed due to poor coverage of the seed layer, the loss of conductivity of the exposed parts can be avoided. That is, the specific resistance of the barrier layer is sufficiently low, e.g., Ru oxide $\leq$ 35 $\mu\Omega$·cm, such that even when portions of the barrier layer are exposed through the seed layer and the barrier layer is oxidized in the exposed regions an increase of the wiring resistance due to the oxidation of the barrier film can be prevented. Further, when electroplating is employed to form the conductive film within a recess, e.g., a via hole or wiring trench, the generation of filling defects is prevented since the conductive film can be formed on either the seed layer or barrier layer, as described in the instant specification, at page 17, lines 7-12, and page 19, lines 1-24.

In contrast, the Soininen et al reference teaches forming a conductive thin film between a substrate and a conductive film using atomic layer deposition (ALD) to prevent diffusion of the copper conductive film, improve film coverage and uniformity over a large area, and improve the adhesion of the deposited film. Specifically, Soininen et al teach depositing a thin conductive film by depositing a metal oxide on a diffusion barrier layer, i.e., TaN, using ALD. The metal oxide is then reduced to a thin metal film which is then used as the seed layer for an electroplating process. The process of Soininen et al does not deposit a "barrier metal film of a metal film of a metal whose conductivity will not be lost when the metal is oxidized" as set forth in claim 21, but instead teaches the Ru or Ir film (converted from an oxide) to be the seed layer on top of a barrier layer (see last sentence of paragraph [0069] and Figure 1, element 16) for electroplating the copper wiring. This methodology is distinctly different from the presently claimed invention set forth in claims 21 and 35.

Specifically, Soininen et al teach the use of TaN as the barrier film 14 and the "conductive thin film" is used as the seed layer 16. The "conductive thin film" is exemplified as Re, Ru, Os, Co, Rh, Tr, Ni, Pd, Pt, Cu, Ag, or Au (see paragraph [0045]). Since, in the embodiments taught by Soininen et al, a TaN barrier layer is used, the specific resistance of which can be as high as 200-300 $\mu\Omega$·cm, the resistance value of the wiring increases. As a result, poor electroplating coverage results in the exposed areas of the seed layer.

The seed layer of Soininen et al serves as an undercoating film used during the electroplating of the upper conductive film. However, since electrodes in an electroplating process are normally applied to an edge (end) of a wafer for establishing an electric field over the entire wafer, it is difficult to electroplate a conductive film in regions of the wafer space far from the electrode, i.e., it is difficult to electroplate in the central region of a wafer. Consequently, if the resistance value of a undercoating seed layer is high, then the voltage applied to the central region of the wafer is decreased

which adversely affects the growth of the electroplated film in the central region of the wafer. Further, if the material of the seed layer and electroplated conductive film are significantly different, then an interface compound of an entirely different compound will be formed during the electroplating which will also adversely affect the uniformity of the growth of the conductive film due to changes in the voltage applied caused by the interface compound.

Since the presently claimed invention set forth in claim 35 requires that the "seed layer is composed of the same metal as the conductive film," Soininen et al also fail to teach or suggest this feature. The patentees instead form the seed layer 16 of an oxide of a metal, i.e., Re, Ru, Os, Co, Rh, Tr, Ni, Pd, Pt, Cu, Ag, or Au (see paragraph [0058]) and therefore fail to appreciate the importance of selecting the electroplated conductive film 18 to be the same material as the seed layer.

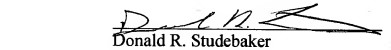
Clearly, the Soininen et al reference does not teach a "barrier metal film of a metal whose conductivity will not be lost when the metal is oxidized" of claim 21 or a "barrier metal film composed of a conductive metal oxide" of claim 35. Nor do the patentees teach following the barrier metal film with the step of "forming a seed layer in contact with the barrier metal film" of claims 21 and 35, "wherein the seed layer is composed of the same metal as the conductive film" as presently claimed in claim 35. Additionally, Soininen et al do not suggest to replace the TaN barrier layer (Figure 1, element 14) with a seed layer of Ru or Ir. Therefore, the Soininen et al reference no longer anticipates the claimed invention and a *prima facie* case of obviousness based upon the teachings of the Soininen et al reference has not been established. Consequently the rejections of claims 21, 22 and 24-27, under either § 102 or § 103, are no longer appropriate and must be withdrawn.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicants' representative,

then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Lastly, it is noted that a separate Petition for Extension of Time (two months) accompanies this response along with a check in payment of the requisite extension of time fee. However, should that petition become separated from this Amendment, then this Amendment should be construed as containing such a petition. Likewise, any overage or shortage in the required payment should be applied to Deposit Account No. 19-2380 (740819-616).

Respectfully submitted,



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MARKED UP VERSION OF THE AMENDMENTS

IN THE CLAIMS:

Please cancel claims 23, 25-31 in their entirety without prejudice or disclaimer of the subject matter disclosed therein.

Please amend claims 21, 22, 24 and 32 as follows.

21. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming, on [a substrate] an underlying wiring, a barrier metal film of a metal whose conductivity will not be lost when the metal is oxidized [or of a conductive metal oxide];

forming a seed layer in contact with the barrier metal film; and

forming a conductive film as [a] an upper-layer wiring, such that conductive film is in contact with the [barrier metal film] seed layer.

22. (Amended) The method of Claim 21, wherein the metal whose conductivity will not be lost when the metal is oxidized is Ru, Ir or an alloy containing Ru or Ir.

24. (Amended) The method of Claim 21, wherein the seed layer [conductive film] is composed of copper or a copper alloy.

32. (Amended) The method of Claim 21 further comprising the step of, after forming the conductive film, forming [a wiring of the conductive film] the upper-layer wiring by etching the conductive film using a mask pattern covering a wiring forming region.